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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,594	08/19/2003	Nobuyasu Kanekawa	056207.50307C1	2784
23911	7590	11/17/2004	EXAMINER	
CROWELL & MORING LLP INTELLECTUAL PROPERTY GROUP P.O. BOX 14300 WASHINGTON, DC 20044-4300			DICKEY, THOMAS L	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,594	KANEKAWA ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 September 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 15-18 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 15, 17 and 18 is/are rejected.
- 7) Claim(s) 16 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 19 August 2003 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. 09/943,384.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. The amendment filed on 09/30/2004 has been entered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of

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NEMOTO et al. 6,407,432 is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

A. Claims 15 and 18 are rejected under 35 U.S.C. § 102(b) as being anticipated by YUKUTAKE et al. (WO 9844687 A1).

Yukutake et al. discloses a semiconductor device, comprising an embedded insulation layer 232 formed in a semiconductor substrate 231; a plurality of power semiconductor elements 215-216-218 formed on said semiconductor substrate 231; a trenches 206-1 through 206-6 isolating between said plurality of power semiconductor elements 215-216-218 formed on said semiconductor substrate 231 on said embedded insulation layer 232, whereby said plurality of semiconductor elements 215-216-218, (groups of said plurality of semiconductor elements each being surrounded by one of the trenches 206-1 through 206-6) are individually isolated from each other; an isolator 207 insulating and driving control electrodes of said power semiconductor elements 215-216-218; and wherein said plurality of power semiconductor elements 215-216-218 are each connected to multiple device terminals in order to provide connectability to said semiconductor device, wherein said plurality of power semiconductor elements 215-216-218 have an input control circuit 213-214-217 supplying a control signal of a specific control pattern to said control electrodes of said plurality of power semiconductor elements 215-216-218 on the base of input signals.

Note, for example, figures 8a and 8b of Yukutake et al.

B. Claim 15 is rejected under 35 U.S.C. § 102(e) as being anticipated by NEMOTO et al. (6,407,432).

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Nemoto et al. discloses a semiconductor device, comprising an embedded insulation layer (not shown in the plan view of figure 19, see insulation layer 10 in cross-section view figure 2 of equivalent embodiment) formed in a semiconductor substrate 1; a plurality of power semiconductor elements 67-68-69 formed on said semiconductor substrate 1; a trench (no part # in figure 19, seen as three regions separately surrounding each element 67-68-69, the equivalent trenches in the embodiment of figure 1 are marked 6a) isolating between said plurality of power semiconductor elements 67-68-69 formed on said semiconductor substrate on said embedded insulation layer, whereby said plurality of semiconductor elements 67-68-69 are individually isolated from each other; an isolator 4 (Nemoto et al.'s figure 19 discloses three isolators 4, the claimed isolator reads on any single one of them) insulating and driving control electrodes (not shown, see page 7 lines 25-27 for the description of the MOSFETS containing the control electrodes) of said power semiconductor elements 67-68-69; and wherein said plurality of power semiconductor elements 67-68-69 are each connected to multiple device terminals (no part # in figure 19, seen as nine cross-hatched regions on the left of figure 19, the equivalent terminals in the embodiment of figure 1 are marked 5a) in order to provide connectability to said semiconductor device. Note figure 19 and column 20 lines 14-34 of Nemoto et al. Note that figure 19 and column 20 lines 14-34 show a specific embodiment that shares common parts (some having part #s in the generic embodiment but not in the specific embodiment of figure 19) with the generic embodiment shown in figures 1-4 and column 6 lines 40-49,55-67, column 7 lines 1-28 and 40-67, and column 8 lines 1-48 of Nemoto et al.

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Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claim 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over NEMOTO ET AL. (6,407,432) in view of MIURA (4,993,396).

Nemoto et al. discloses a semiconductor device with all the limitations of claim 16 except an ignition coil driven by the power semiconductor elements. Not Note figure 19 and column 20 lines 14-34 of Nemoto et al.

However, Miura discloses a semiconductor device with an ignition coil 2 driven by power semiconductor element 1. Note figure 1 and column 4 lines 27-46 of Miura. Therefore, it would have been obvious to a person having skill in the art to use the power semiconductor elements of Nemoto et al.'s semiconductor device to drive an ignition coil such as taught by Miura because power semiconductor elements have a faster rise time and generate higher voltages into inductive loads such as ignition coils.

B. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over NEMOTO et al. (6,407,432) in view of FOERSTER (5,828,141).

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Nemoto et al. discloses a semiconductor device with all the limitations of claim 16 except a fuel injector driven by the power semiconductor elements. Note figure 19 and column 20 lines 14-34 of Nemoto et al..

However, Foerster discloses a semiconductor device with a fuel injector driven by power semiconductor elements. Note figure 1 and column 1 lines 32-35 of Foerster. Therefore, it would have been obvious to a person having skill in the art to having skill in the art to use the power semiconductor elements of Nemoto et al.'s semiconductor device with the fuel injector driven by power semiconductor elements such as taught by Foerster in order to demagnetize the inductive load presented by the fuel injector as rapidly as possible, in a repeatable fashion.

Response to Arguments

5. Applicant's arguments filed 09/30/2004 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 15-17 have been considered but are moot in view of the new ground(s) of rejection.

With respect to claims 15 and 18 it is argued, at page 6 of the remarks, that "The circuit units of the '687 reference each contain a plurality of elements together and they are isolated from another plurality of elements by the trench, [in contrast to] the present invention [which] by forming the trench between semiconductor elements (transistors), each semiconductor element is individually isolated from the other semiconductor element."

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Examiner's response is two-fold. First, applicant seems to assume that the term "element" has a fairly flexible definition – broad enough to read on a transistor (which most having skill in the art would assume to have at least three parts, namely source, channel and drain), but narrow enough so that a four part entity, say a transistor attached to a MOS capacitor, would consist of two "elements." Such a definition does not appear to be supported by the application as filed. Second, and more fatally, applicant ignores the fact that claims 15 and 18 are *open-ended*, that is to say, the claimed device comprises the recited elements but does not exclude others. Say, for example, the '687 reference discloses (as seems to be the case) a device having at least four "elements," named, for convenience, "Moe," "Curly," "Larry," and "Shemp." Further, elements Larry and Shemp are "individually isolated" from each other. In such case Larry and Shemp form a plurality (at least two) of elements, and each (Larry or Shemp) of said elements is "individually isolated from the other (Shemp or Larry) semiconductor element." Relationships between Moe and Shemp, or between Curly and Larry (and indeed even the existence or non-existence of either Moe or Curly or any other disclosed feature) are moot.

With respect to claims 15 and 18 it is further argued, at page 6 of the remarks, that "When the semiconductor elements are connected in series, the withstand voltage can be raised. In contrast, the purpose of Yukutake [the '687 reference] is to decrease the number of parts, decrease the weight and the cost as well as prevent deterioration in the frequency band caused by an isolation transform which is eliminated according to Yukutake." In response to applicant's argument that the references fail to show certain features of

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applicant's invention, it is noted that the features upon which applicant relies (i.e., to increase withstand voltage without decreasing the number of parts, or the weight, or the cost, or prevent deterioration in the frequency band) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
11/2004

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Primary Examiner
Art Unit 2826